General Information

Title:	ECE/CS 5710/6710 - Digital VLSI Design - Fall 2018
Units:	4 credits
Instructor:	Pierre-Emmanuel Gaillardon: pierre-emmanuel.gaillardon@utah.edu, MEB 2126
Classes:	Tue & Thu 2:00pm - 3:20pm, M LI 1130
Office Hours:	by appointment
Lead TA - Grader:	Edouard Giacomin (Lead TA - Grader): edouard.giacomin@utah.edu
Lab TA:	Tannu Sharma (Labs): tannu.sharma@utah.edu
Lab Hours:	Mon & Fri 4pm - 5pm in CADE, and by appointment
Required Text Book:	*Principles of CMOS VLSI Design: A Systems Perspective* By Weste & Harris
Prerequisites:	ECE/CS 3700

Course Description

This is the introductory course in VLSI where you will learn how to drive Electronic Design Automation (EDA) Computer-Aided Design (CAD) tools. With them you will learn the physical mask design for transistors and how to create and characterize your own logic gates. You will then use commercial cell libraries to design a complete integrated circuit architecture including power delivery and bonding pads.

Many aspects of Digital VLSI design will be introduced in order to take this significant and enjoyable design journey. However, note that *this is not a course in digital system design or computer architecture*. You will already need to know Verilog, Boolean logic, and how to design and implement combinational and sequential digital circuits (such as adders and other datapath logic, and finite state machines). The project will also require some knowledge of computer architecture for you to complete a moderately large digital design. We recommend you take ECE/CS 3810 (Computer Architecture) before this course.

Topics that will be covered in lectures include:

- Basic transistor theory
- CMOS processes
- VLSI CAD tools
- Mask layout methods and design rules
- Circuit simulation and characterization
- Custom datapath design
- Design validation
- Full chip assembly

The class will require extensive use of CAD tools. All of the CAD tools required will be available in the CADE lab. Students must have an account that will allow them to use the CADE machines. These tools *do not* run on MS Windows. Therefore some familiarity with various versions of Unix (such as Linux or Solaris) and the X window system is required for this course.

You will be guided through the tools through complete lab manuals and you will receive the aid of the TA in the labs and project. However, there is no specific lab class that you are required to attend. You can perform the labs and your project at your own convenience, either in the CADE lab at the University, or across the network. Remember that nothing can replace taking the time to read the CAD tool documentation.

Integrated circuit design is mastered only through experience, so this is a hands-on course with lots of labs and project time. The homework, as well as lectures, will be closely tied to a series of labs where you will get a basic training in full-custom and semi-custom design and then you will put this in practice with a personal project of your choice. The final library and project will be done in teams (preferably made up of 3 to 4 students). The initial labs will be done individually. You must submit your lab reports. You are encouraged to interact with others, but until you are asked to form teams, the work on your cell designs, simulations, etc., must be independent and fully your own work.

Fabrication of your final project is possible thanks to the research funding provided through the MOSIS service. Few tasks are more rewarding than creating a functional integrated circuit. However, few tasks are also more disappointing that spending time on the design of an integrated circuit only to have the fabricated circuit return non-functional. Therefore, careful design practices must be followed if you are to fabricate your chip including sufficient Design-For-Test, validation of your design, and a quality design review. If you do fabricate the chip, you will be required to take ECE/CS 6712 in the spring to test and report on the results. 6712 is a fun class and a reward to those who make the effort to fabricate their designs.

Required Textbook:

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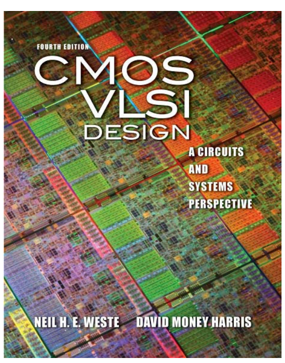
<td>
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<td></td>
<td>Principles of CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), By Neil Weste and David Harris. Published by Addison-Wesley, c2010, ISBN 0-321-54774-8.
Get the errata (mistakes) for the textbook.</td>
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Additional Recommended Textbooks:

Logic Effort - designing fast CMOS Circuits, I. Sutherland, B. Sproull, and D. Harris. Academic Press, 1999

Analysis and Design of Digital Integrated Circuits (3rd ed), David Hodges. McGraw Hill, 2004.

Modern VLSI Design (3rd ed), Wayne Wolf. Prentice Hall, 2002.

Digital Integrated Circuits (2nd ed), Jan M. Rabaey. Prentice Hall, 2003.

The Design and Analysis of VLSI Circuits, Glasser and Doberpuhl. Addison-Wesley, 1985. *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, by Erik Brunvand. Published by Addison-Wesley,

c2010 ISBN 978-0321547996
Note: The there is an update for the book to map from the version 5 to version 6 of the Cadence design tool interfaces. *You will need to use this in conjunction with the book to efficiently use the tools.*

Policies

- The college of Engineering guidelines.
- Incomplete policy: You can't get an incomplete unless you have a documented medical or legal emergency.
- Add/Drop policy: The standard University Policy is applied.
- Late submission: We follow a strict late submission rule based on the timestamp on your Canvas submission. Late submissions are at risk to not be graded and result in a 0% score. If graded, late homework/reports submissions will be handled as follow: Between due date and 1 week after the submission, the maximum achievable grade will be reduced to 75%. Further late submissions will have a maximum achievable grade of 50%. The instructor reserves the right to reject any late submissions. If you have any concerns, start early or inform the instructor! Any changes in due date will affect the entire class at the discretion of the lecturers.
- The instructor reserves the right to add/remove exams/graded assignments and/or change deadlines at his discretion.
- The University of Utah seeks to provide equal access to its programs, services and activities for people with disabilities. If you will need accommodations in the class, reasonable prior notice needs to be given to the Center for Disability Services, 162 Olpin Union Building, 801-581-5020. CDS will work with you and the instructor to make arrangements for accommodations. All written information in this course can be made available in alternative format with prior notification to the Center for Disability Services.
- The University of Utah's Student Code covers cheating and other student conduct policies.
- ECE Cheating policy: ECE students are bound by the ECE Academic Misconduct Policy as well as the University's Student Code. Cheating on exams (using unauthorized materials, copying or collaborating with another student), and plagiarizing (copying words, code, or work from another person without crediting it to them), constitute academic misconduct in this course and will result in academic sanction. Academic misconduct on any assignment may result in a sanction in this course up to failing the course.

Grading Policy:

Labs and Homework	40%
Final Design Review	5%
Written Exam:	15%
Project (design and report):	40%

The **homework** will take the form of problem sets, project proposals, and other written work. The **Labs** will involve using the VLSI CAD tools to design the mask work and layout of cells that will be used in your project. The class **project** will require the design of a small digital standard cell library that will then be used as a cell library for a moderate sized functional design. Class members will join design teams for the implementation of the design. The **design review** will consist of a short presentation of the project to the class. The **project report** will be a paper in conference or journal format.

Those taking the graduate level course will have additional requirements that include a more rigorous project or design flow and the review of one or more papers relating to VLSI from journals or conferences in the area. These could be related to the project being implemented.

Detail on the requirements for your project reports will be provided later - but have to comply with the MOSIS requirements.

Tentative Schedule:

(This is my best guess at initial schedule based on previous offerings of this course. Things are likely to change a little during the semester...) Slide links will become live as the class goes forward...

Date	Lecture	Concurrent Lab/Homework	Additional Readings
Aug. 21	Lecture 1: Introduction to Digital VLSI Design		
Aug. 23	Lecture 2: MOSFETs Fundamentals		
Aug. 28	Lecture 3: Inverter DC and Transient Characteristics	Homework 1: Review of Basic Digital Design Skills	
Aug. 30	Lecture 4: CAD Flow and Introduction to Layout		
Sep. 4	Lecture 5: Combinational Circuit Design	Lab 1: CMOS Inverter - Schematic and Circuit Simulation	
Sep. 6	Lecture 6: Circuit Families		
Sep. 10	Lecture 7: Sequential Circuit Design	Lab 2: CMOS Inverter - Physical Design	
Sep. 13	Lecture 8: Logical Effort		
Sep. 18	Lecture 9: Logical Effort - cont'd	Lab 3: D Flip-Flop	
Sep. 20	Lecture 10: MIPS Flow and Intro to Semi-custom Toolsuites		
Sep. 25	Lecture 11: Power	Lab 4: Logic Synthesis and Front-end Flow	
Sep. 27	Lecture 12: Wires		
Oct.	Lecture 13: Project Ideas	Lab 5: Floorplanning and Back-end	

2		Flow	
Oct. 4	No class		
Oct. 9	FALLBREAK		
Oct. 11	FALLBREAK		
Oct. 16	Lecture 14: Scaling	Project	
Oct. 18	Lecture 15: Reliability		
Oct. 23	Lecture 16: Design for Testatibility	Project	
Oct. 25	Lecture 17: Adders		
Oct. 30	Lecture 18: Datapath Design	Project	
Nov. 1	Q&A Session		
Nov. 6	Exam	Project	
Nov. 8	Lecture 19: Memories		
Nov. 13	Lecture 20: Packaging	Project	
Nov. 15	Lecture 21: PLL/DLL		
Nov. 20	Lecture 22: I/Os	Project	
Nov. 22	THANKSGIVING		
Nov. 27	Project Q&A	Project	
Nov. 29	Project Q&A		
Dec. 4	Project Presentations		
Dec. 6	Project Presentations		